REMARKS

Claim 4 is canceled. New claims 50-57 are added. Support for the new claims is provided by exemplary embodiments of the invention described at, for example, pages 6-7 of the originally-filed application.

Claims 1, 2 and 4 are rejected under 35 U.S.C. §102(b) as being anticipated by Dennison et al (U.S. Patent No. 5,272,367).

Regarding an anticipation rejection, the Examiner is respectfully reminded that the Federal Circuit provides that §102 anticipation requires that *each and every element* of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990); MPEP §2131 (8th ed. revision no. 2). The corollary of this rule is that the absence from a cited §102 reference of *any* claimed element negates the anticipation. *Kloster Speedsteel AB, et al. v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 recites conducting second type halo implants into the first type MOS transistors in less than all *peripheral* MOS transistors of the first type, wherein the conducting of the second type **halo implants** includes conducting said implants into *only one* of the **source and drain regions**. That is, the subject matter is directed to at least one *peripheral* transistor having respective source/drain regions wherein one of the regions has a halo implant and the other region does not have a halo implant. Dennison teaches only a single peripheral transistor having a halo implant, and that halo implant is **in both** the source **and** drain regions of the peripheral transistor (Figs. 5 and 6; col. 7, lns. 49+).

Accordingly, it is inconceivable that Dennison teaches or suggests conducting second type halo implants into the first type MOS transistors in less than all *peripheral* MOS transistors of the first type, and wherein the conducting of the second type halo implants ... **into only one** of the source and drain regions as positively recited by claim 1. For at least this reason, claim 1 is allowable.

Moreover, claim 1 recites the **peripheral circuitry** comprises first *and* second type MOS transistors and conducting second type halo implants into the first type MOS transistors **in less than all** peripheral MOS transistors. Accordingly, the subject matter of claim 1 is at least directed to different processing (halo implants) between more than one peripheral transistor. However, Dennison teaches a halo implant with respect to **only one** peripheral transistor (Fig. 5; col. 7, lns. 52-58) and does not provide any teachings to a second peripheral transistor. Consequently, Dennison fails to teach or suggest conducting second type halo implants into the first type MOS transistors **in less than all** peripheral MOS transistors as positively recited in claim 1. Claim 1 is allowable.

Claim 2 depends from independent claim 1, and therefore, is allowable for the reasons discussed above with respect to the independent claim, as well as for its own recited features which are not shown or taught by the art of record.

For example, claim 2 recites the second type is p-type wherein claim 1 from which claim 2 depends recites conducting second type halo implants into the first type MOS transistors. That is, claim 2 is directed to halo implants that are p-type. However, Dennison explicitly teaches a halo implant that is n-type: "this forms an n-type phosphorous 'halo' implant to improve short channel PMOS device performance" (col. 7, lns.62-64), and this is the only teaching to a halo implant presented by Dennison. Therefore, Dennison fails to teach or suggest conducting second type halo implants into

the first type MOS transistors and the second type being p-type as positively recited by claim 2. Claim 2 is allowable.

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to phone the undersigned at any time in the event that the next Office Action is one other that a Notice of Allowance.

Respectfully submitted,

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